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4. **Designing phase locked oscillators for synchronization**
Rich, M.;
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Volume 21, Issue 4, Jul 1974 Page(s):466 - 472
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Goering, R.; Krolikoski, S.J.;
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21-25 June 1999 Page(s):999 - 1000
AbstractPlus | Full Text: PDF(128 KB) IEEE CNF

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Krolikoski, S.J.; Schirrmeister, F.; Salefski, B.; Rowson, J.; Martin, G.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International S
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1 Post-layout transistor sizing for power reduction in cell-based design
Masanori Hashimoto, Hidetoshi Onodera
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(104.00 KB) Additional information: full citation, abstract, references, index terms

In this paper, we propose a skew-programmable clock-routing architecture. The skews can be adjusted using programmable delay elements (*PDEs*) which we insert into the clock trees. We develop efficient, shortest-path-based algorithms for programming *PDEs* to optimize timing. Unlike previous methods for *FPGA* skew optimization which require large power and routing penalty, our method can achieve large timing improvement with small overhead. Typically, if timing requirements are t ...

Keywords: clock architecture, placement, skew optimization

6 Post-layout optimization for deep submicron design
Koichi Sato, Masamichi Kawarabayashi, Hideyuki Emura, Naotaka Maeda
June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(1.317.66 KB) Additional information: full citation, references, citings, index terms

7 Design for manufacturability and global routing: Performance-impact limited area fill synthesis
Yu Chen, Puneet Gupta, Andrew B. Kahng
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(98.72 KB) Additional information: full citation, abstract, references, citings, index terms

Chemical-mechanical planarization (CMP) and other manufacturing steps in very deep-submicron VLSI have varying effects on device and interconnect features, depending on the local layout density. To improve manufacturability and performance predictability, area fill features are inserted into the layout to improve uniformity with respect to density criteria. However, the performance impact of area fill insertion is not considered by any fill method in the literature. In this paper, we first revie ...

Keywords: VLSI manufacturability, coupling capacitance extraction, dummy fill problem, greedy method, linear programming, signal delay

8 Architecture analysis and automation: Architecture evaluation for power-efficient FPGAs
Fei Li, Deming Chen, Lei He, Jason Cong
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(254.57 KB) Additional information: full citation, abstract, references, citings, index terms

This paper presents a flexible FPGA architecture evaluation framework, named fpgaEVA-LP, for power efficiency analysis of LUT-based FPGA architectures. Our work has several contributions: (i) We develop a mixed-level FPGA power model that combines switch-level models for interconnects and macromodels for LUTs; (ii) We develop a tool that automatically generates a back-annotated gate-level netlist with post-layout extracted capacitances and delays; (iii) We develop a cycle-accurate power simulato ...

Keywords: FPGA architecture, FPGA power model, low power design

9 Post-layout optimization of power and timing for ECL LSIs
A. Onozawa, H. Kitazawa, K. Kawai
March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available: pdf(583.61 KB) Additional information: full citation

Keywords: ECL LSIs, bipolar ECL LSI, bipolar logic circuits, circuit CAD, circuit optimisation, delay time, emitter-coupled logic, integrated circuit design, integrated circuit modelling, large scale integration, logic CAD, nonlinear programming, nonlinear programming solver, optimization algorithm, post-layout optimization, power dissipation, switching current, timing

10 Poster Paper Introductions: Crosstalk noise optimization by post-layout transistor sizing
Masanori Hashimoto, Masao Takahashi, Hidetoshi Onodera
April 2002 **Proceedings of the 2002 international symposium on Physical design**

Full text available: pdf(157.73 KB) Additional information: full citation, abstract, references, citings, index terms

This paper proposes a post-layout transistor sizing method for crosstalk noise reduction. The proposed method downsizes the drivers of the aggressor wires for noise reduction, utilizing the precise interconnect information extracted from the detail-routed layouts. We develop a transistor sizing algorithm for crosstalk noise reduction under delay constraints, and construct a crosstalk noise optimization method utilizing a crosstalk noise estimation method and a transistor sizing framework

which a ...

Keywords: capacitive coupling noise, crosstalk noise, gate sizing, post-layout optimization, transistor sizing

11 Post-layout timing-driven cell placement using an accurate net length model with movable Steiner points
Amir H. Ajami, Massoud Pedram
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

This paper presents a new algorithm for timing-driven cell placement using the notion of movable Steiner points that capture the net topology. The proposed algorithm improves the timing closure at the backend of the EDA design flow. Unlike conventional flows that perform placement and routing in two separate steps and use rough estimates of the net lengths during placement, our algorithm uses accurate net lengths by considering the net topologies during the Elmore delay calculation step and ...

12 Integrating logic retiming and register placement
Tzu-Chieh Tien, Hsiao-Pin Su, Yu-Wen Tsay, Yih-Chih Chou, Youn-Long Lin
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

13 Filling and slotting: analysis and algorithms
Andrew B. Kahng, Gabriel Robins, Anish Singh, Huijuan Wang, Alexander Zelikovsky
April 1998 **Proceedings of the 1998 international symposium on Physical design**

In very deep-submicron VLSI, certain manufacturing steps &mdash notably optical exposure, resist development and etch, chemical vapor deposition and chemical-mechanical polishing (CMP)&mdash have varying effects on device and interconnect features depending on local characteristics of the layout. To make these effects uniform and predictable, the layout itself must be made uniform with respect to certain density parameters. Traditionally, only foundries have performed the p ...

14 IDA: interconnect delay analysis for integrated circuits
A. J. de Geus, J. B. Reed, M. Rekhson, G. Wikle
June 1984 **Proceedings of the 21st conference on Design automation**

A delay analysis program has been developed to compute the signal propagation delays attributed to RC interconnection nets in integrated circuits. To take into account the bidirectional nature of MOS transmission gates, the program simulates nets connected through transmission gates as single entities refered to as "supernets". In order to obtain a single set of realistic lumped delays for nets with transmission gates, a delay path analysis and reduction algorithm is used.

15 Propagation delay calculation for interconnection nets on printed circuit boards by reflected waves
Heinz Mattes, Wolfgang Weisenseel, Gerhard Bischof, Reimund Dachauer
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

16 Design strategies for active power reduction: UDSM (ultra-deep sub-micron)-aware post-layout power optimization for ultra low-power CMOS VLSI
Kyu-won Choi, Abhijit Chatterjee
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

In this paper, we propose an efficient approach to minimize total power (switching, short-circuit, and leakage power) without performance loss for ultra-low power CMOS circuits in nanometer technologies. We present a framework for combining supply/threshold voltage scaling, gate sizing, and interconnect scaling techniques for power optimization and propose an efficient heuristic algorithm which ensures that the total slack budget is maximal and the total power is minimal in the presence of back ...

Keywords: device and interconnect co-optimization, low-power design, nanometer design, time slack distribution

17 Advances in FPGA CAD: The effect of post-layout pin permutation on timing
Yuzheng Ding, Peter Suaris, Nanchi Chou
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**

In this paper we study the effect of post-layout pin permutation of designs for FPGA devices with non-uniform cell delays. We present a simple, but timing optimal, pin permutation scheme, and report the results of applying the scheme on a set of public logic synthesis benchmark designs that were synthesized and placed by state-of-the-art commercial FPGA design tools configured to maximum optimization level. Despite the preceding optimizations, we still observed an average timing improvement of 3 ...

Keywords: FPGA, logic synthesis, placement, timing optimization

18 Fast module mapping and placement for datapaths in FPGAs
Timothy J. Callahan, Philip Chong, André DeHon, John Wawrzynek
March 1998 **Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays**

By tailoring a compiler tree-parsing tool for datapath module mapping, we produce good quality results for datapath synthesis in very fast run time. Rather than flattening the design to gates, we preserve the datapath structure; this allows exploitation of specialized datapath features in FPGAs, retains regularity, and also results in a smaller problem size. To further achive high mapping speed, we formulate the problem as tree covering and solve it efficiently with a linear-time dynamic pr ...

19 MIDAS: integrated CAD for total system design
W. M. Budney, S. K. Holewa
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Control Data's Modular Integrated Design Automation System (MIDAS) is a highly integrated CAD system supporting the full range of activities required for the design of complex digital systems. From schematic capture through design verification and manufacturing, MIDAS emphasizes a structured top down approach, from chips to supercomputers. MIDAS is fully hierarchical and is capable of managing and controlling the design of some of the world's largest computers, as well as speeding up the de ...

20 VAMP: a VHDL based concept for accurate modeling and post layout timing simulation of electronic systems
Bernhard Wunder, Gunther Lehmann, Klaus D. Müller-Glaser
June 1990 **Proceedings of the 33rd annual conference on Design automation**

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1 DA STANDARDS ACTIVITIES
April 1989 **ACM SIGDA Newsletter**, Volume 19 Issue 1
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract

Dr. Jim Armstrong from Virginia Polytechnic Institute (VPI) called to order the third meeting of the VHDL modeling subcommittee of the IEEE DATC on January 12 at MCC in Austin, Texas. This meeting was held jointly with the Electronic Industry Association (EIA). The meeting was started by recounting what had taken place at the previous two meetings. He detailed the approach taken by the group to develop a model standard. Four papers will be published in a special issue of Design & Test ma ...

2 Architecture analysis and automation: Architecture evaluation for power-efficient FPGAs
Fei Li, Deming Chen, Lei He, Jason Cong
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Full text available: pdf(338.83 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a flexible FPGA architecture evaluation framework, named fpgaEVA-LP, for power efficiency analysis of LUT-based FPGA architectures. Our work has several contributions: (i) We develop a mixed-level FPGA power model that combines switch-level models for interconnects and macromodels for LUTs; (ii) We develop a tool that automatically generates a back-annotated gate-level netlist with post-layout extracted capacitances and delays; (iii) We develop a cycle-accurate power simulato ...

Keywords: FPGA architecture, FPGA power model, low power design

3 VHDL: a call for standards
David R. Coelho
June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**
Full text available: pdf(695.25 KB) Additional Information: full citation, abstract, references, citings, index terms

With the introduction of the IEEE 1076 version of VHDL, an excellent industry standard hardware description language is now available. VHDL is an extremely flexible and versatile language. As a consequence, the language reference documentation is not sufficient to

insure that models written by one hardware designer will be compatible with another's models. What is required is a set of VHDL modelling conventions and standard packages which structure the usage of VHDL modelling approaches. Th ...

4 Optimization of custom MOS circuits by transistor sizing
Andrew R. Conn, Paula K. Coulman, Ruud A. Haring, Gregory L. Morrill, Chandu Visweswariah
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(68.85 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Optimization of a circuit by transistor sizing is often a slow, tedious and iterative manual process which relies on designer intuition. Circuit simulation is carried out in the inner loop of this tuning procedure. Automating the transistor sizing process is an important step towards being able to rapidly design high-performance, custom circuits. JiffyTune is a new circuit optimization tool that automates the tuning task. Delay, rise/fall time, area and power targets are accommodated. Each (weig ...

Keywords: Circuits, transistor sizing, optimization, simulation, gradients.

5 Modeling ASIC memories in VHDL
E. Balaji, P. Krishnamurthy
September 1996 **Proceedings of the conference on European design automation**
Full text available: pdf(85.09 KB) Additional Information: full citation, references, index terms

6 Timing abstraction: Automated timing model generation
Ajay J. Daga, Loa Mize, Subramanyam Sripada, Chris Wolff, Qiuyang Wu
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(260.13 KB) Additional Information: full citation, abstract, references, index terms

The automated generation of timing models from gate-level netlists facilitates IP reuse and dramatically improves chip-level STA runtime in a hierarchical design flow. In this paper we discuss two different approaches to model generation, the design flows they lend themselves to and results from the application of these model generation solutions to large customer designs.

Keywords: EDA, model generation, static timing analysis

7 Design methodology of a 200MHz superscalar microprocessor: SH-4
Toshihiro Hattori, Yusuke Nitta, Mitsuho Seki, Susumu Narita, Kunio Uchiyama, Tsuyoshi Takahashi, Ryuichi Satomura
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(282.85 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

A new design methodology focusing on high speed operation and short design time is described for the SH-4 200MHz superscalar microprocessor. Random test generation, logic emulation, and formal verification are applied to logic verification for shortening design time. Delay budgeting, forward/back annotation, and clock design are key features for timing driven design.

Keywords: design methodology, microprocessor, timing, verification

8 Multi-objective circuit partitioning for cutsize and path-based delay minimization
Cristinel Ababei, Navaratnasothie Selvakkumaran, Kia Bazargan, George Karypis
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(466.96 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present multi-objective hMetis partitioning for simultaneous cutsize and circuit delay minimization. We change the partitioning process itself by introducing a new objective function that incorporates a truly path-based delay component for the most critical paths. To avoid semi-critical paths from becoming critical, the traditional slack based delay component is also included in the cost function. The proposed timing driven partitioning algorithm is built on top of the hMetis al ...

9 DA STANDARDS ACTIVITIES
July 1988 **ACM SIGDA Newsletter**, Volume 18 Issue 2
Full text available: pdf(1.01 MB) Additional Information: full citation, abstract

Users of electronic design automation (EDA) systems often discover that their different tools don't talk to each other. Each tool has its own way of expressing design data and these ways are often incompatible.

10 Session 10: Regular Circuit Fabrics (invited): Architecture and synthesis for multi-cycle communication
Jason Cong, Yiping Fan, Xun Yang, Zhiru Zhang
April 2003 **Proceedings of the 2003 international symposium on Physical design**
Full text available: pdf(314.81 KB) Additional Information: full citation, abstract, references, citings, index terms

For multi-gigahertz designs in nanometer technologies, data transfers on global interconnects take multiple clock cycles. In this paper, we propose a *regular distributed register* (RDR) micro-architecture for multi-cycle on-chip communication. An RDR architecture structurally consists of a two-dimensional array of islands, each of which contains a cluster of computational logic and local register files. We also propose a new synthesis methodology based on the RDR architecture. Novel layout ...

Keywords: RDR, binding, deep sub-micron, interconnect, multi-cycle communication, placement, scheduling, timing closure

11 Integrating logic retiming and register placement
Tzu-Chieh Tien, Hsiao-Pin Su, Yu-Wen Tsay, Yih-Chih Chou, Youn-Long Lin
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(440.79 KB) Additional Information: full citation, references, citings, index terms

12 Advances in FPGA CAD: The effect of post-layout pin permutation on timing
Yuzheng Ding, Peter Suaris, Nanchi Chou
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**
Full text available: pdf(327.46 KB) Additional Information: full citation, abstract, references, index terms

In this paper we study the effect of post-layout pin permutation of designs for FPGA devices with non-uniform cell delays. We present a simple, but timing optimal, pin permutation scheme, and report the results of applying the scheme on a set of public logic synthesis benchmark designs that were synthesized and placed by state-of-the-art commercial FPGA design tools configured to maximum optimization level. Despite the preceding optimizations, we still observed an average timing improvement of 3 ...

Keywords: FPGA, logic synthesis, placement, timing optimization

13 A design flow for partially reconfigurable hardware
Ian Robertson, James Irvine
May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2
Full text available: pdf(698.30 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a top-down designer-driven design flow for creating hardware that exploits partial run-time reconfiguration. Computer-aided design (CAD) tools are presented, which complement conventional FPGA design environments to enable the specification, simulation (both functional and timing), synthesis, automatic placement and routing, partial configuration generation and control of partially reconfigurable designs. Collectively these tools constitute the dynamic circuit switching CAD f ...

Keywords: FPGA, Viterbi decoder, configuration control, dynamically reconfigurable logic (DRL), power estimation, run-time reconfiguration (RTR)

14 Novel design methodologies and signal integrity: Temporofunctional crosstalk noise analysis
Donald Chai, Alex Kondratyev, Yajun Ran, Kenneth H. Tseng, Yosinori Watanabe, Malgorzata Marek-Sadowska
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(177.56 KB) Additional Information: full citation, abstract, references, index terms

Noise affects circuit operation by increasing gate delays and causing latches to capture incorrect values. This paper proposes a method of characterizing correlation of signal transitions in multiple nets by considering both timing and functionality of the signals, and uses it in an analysis procedure to eliminate noise faults that cannot actually happen when such correlations are considered. It uses four-variable Boolean logic to characterize signal transitions in a time interval, and formulate ...

Keywords: SAT formula, crosstalk noise, timed Boolean logic

15 Physical design and synthesis (panel): merge or die!
Richard Bushroe, Massoud Pedram, Raul Camposano, Giovanni De Micheli, Antun Domic, Chi-Ping Hsu, Michael Jackson
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**
Full text available: pdf(63.96 KB) Publisher Site Additional Information: full citation, abstract, citings, index terms

As IC fabrication capabilities extend down to sub-half-micron, the significance of interconnect delay and powerdissipation can no longer be ignored. Existing enhancements to synthesis and physical design tools (such as non-linear delay modeling, custom wire load models, back annotation of calculated delays, early oorplanning, post-layoutre-mapping and resizing) have not been able to solve theproblem. It thus remains that tradeoffs in logical

and physical domains must be addressed in an integrate ...

16 Poster session 1: A practical CAD technique for reducing power/ground noise in DSM circuits
Arindam Mukherjee, Krishna Reddy Dusety, Rajsaktish Sankaranarayan
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**
Full text available: pdf(101.48 KB) Additional Information: full citation, abstract, references, index terms

One of the fundamental problems in Deep Sub Micron (DSM) circuits is Simultaneous Switching Noise (SSN), which causes voltage fluctuations in the circuit power/ground networks. In this work we propose a CAD optimization technique to spread out the switching times of different gates in a circuit to reduce its SSN, by sizing them appropriately. We make sure that its critical delay does not increase while its p/g noise decreases. Our formulation is a Linear Programming one, which we have efficientl ...

Keywords: gate sizing, linear programming, low power, power/ground noise, simultaneous switching noise, timing analysis

17 Post-layout optimization for deep submicron design
Koichi Sato, Masamichi Kawarabayashi, Hideyuki Emura, Naotaka Maeda
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(317.66 KB) Additional Information: full citation, references, citings, index terms

18 Combined topological and functionality based delay estimation using a layout-driven approach for high level applications
Champaka Ramachandran, Fadi J. Kurdahi
November 1992 **Proceedings of the conference on European design automation**
Full text available: pdf(854.38 KB) Additional Information: full citation, references, citings, index terms

19 Verification of a Complex SoC: The PRO3 Case-Study
F. Andritsopoulos, C. Charopoulos, G. Doumenis, F. Karouballs, Y. Mitsos, F. Petreas, I. Theologitou, S. Perissakis, D. Reisis
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2**
Full text available: pdf(363.23 KB) Publisher Site Additional Information: full citation, abstract

In this paper we present the experience gained from the design and verification of a complex network processor. The PRO3 processor1 can operate in either ATM or IP based multiprotocol networking environments, supporting link rates up to 2.4 Gbps. We describe the methodology followed during the verification process, from specifications to silicon prototype test and highlight the problems encountered during the post-layout procedure. To accommodate the application verification a proprietary Debug ...

20 Poster Session 1: Structured interconnect architecture: a solution for the non-scalability of bus-based SoCs
Cristian Grecu, Partha Pratim Pande, André Ivanov, Res Saleh
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**
Full text available: pdf(220.40 KB) Additional Information: full citation, abstract, references, index terms

Multi-Processor (MP-SoC) platforms are emerging as the latest trend in SoC design. Monolithic bus-based interconnect architectures will not be able to support the clock cycle requirements of these high performance SoCs. Systems having multiple smaller buses, integrated through repeaters or bridges, are possible alternatives. But these kinds of solutions are ad-hoc in nature. By adopting a more structured network-based design paradigm, specific clock cycle requirements can easily be met. The prec ...

Keywords: BFT, MP-SoC, bus, pipelining, scalability

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1 Advances in synthesis: Implementing asynchronous circuits using a conventional EDA tool-flow
Christos P. Sotiriou
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(107.01 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an approach by which asynchronous circuits can be realised with a conventional EDA tool flow and conventional standard cell libraries. Based on a gate-level asynchronous circuit implementation technique, direct-mapping, and by identifying the delay constraints and exploiting certain EDA tool features, this paper demonstrates that a conventional EDA tool flow can be used to describe, place, route and timing-verify asynchronous circuits.

Keywords: EDA, asynchronous, tool-flow

2 Testing and Fault-Tolerance: Test generation for resistive opens in CMOS
Arun Krishnamachary, Jacob A. Abraham
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**
Full text available: pdf(100.35 KB) Additional Information: full citation, abstract, references, index terms

This paper develops new techniques for detecting both stuck-open faults and resistive open faults, which result in increased delays along some paths. The improved detection of CMOS open defects is made possible by a new delay fault model which combines the advantages of the gate delay fault model and the path delay fault model. We develop a test generation methodology for this fault model which enables generation of test vectors that test a percentage of the longest sensitizable paths in the des ...

Keywords: defect detection, delay testing, resistive opens

3 A new gate delay model for simultaneous switching and its applications
Liang-Chi Chen, Sandeep K. Gupta, Melvin A. Breuer
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(163.26 KB) Additional Information: full citation, abstract, references, citings, index terms

4 Physical considerations in high-level synthesis: A watermarking system for IP protection by a post layout incremental router
Tingyuan Nie, Tomoo Kisaka, Masahiko Toyonaga
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Full text available: pdf(1.92 MB) Additional Information: full citation, abstract, references, index terms

In this paper, we introduce a new watermarking system for IP protection on post-layout design phase. Firstly the copyright is encrypted by DES (Data Encryption Standard) and then embedded by using an incremental router into the layout design. This watermarking technique uniquely identifies the circuit origin, yet is difficult to be detected or fabricated. The incremental router consists of a rip-up and a special re-router that inserts redundant bends into wires probabilistic. We evaluated the te ...

Keywords: incremental router, intellectual property protection (IPP), post layout design, watermarking

5 A design flow for partially reconfigurable hardware
Ian Robertson, James Irvine
May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2
Full text available: pdf(698.30 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a top-down designer-driven design flow for creating hardware that exploits partial run-time reconfiguration. Computer-aided design (CAD) tools are presented, which complement conventional FPGA design environments to enable the specification, simulation (both functional and timing), synthesis, automatic placement and routing, partial configuration generation and control of partially reconfigurable designs. Collectively these tools constitute the dynamic circuit switching CAD f ...

Keywords: FPGA, Viterbi decoder, configuration control, dynamically reconfigurable logic (DRL), power estimation, run-time reconfiguration (RTR)

6 Session 9A: System level test and reliability: Accurate CMOS bridge fault modeling with neural network-based VHDL saboteurs
Don Shaw, Dhamin Al-Khalili, Côme Rozon
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(137.79 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new bridge fault model that is based on a multiple layer feedforward neural network and implemented within the framework of a VHDL saboteur cell. Empirical evidence and experimental results show that it satisfies a prescribed set of bridge fault model criteria better than existing approaches. The new model computes exact bridged node voltages and propagation delay times with due attention to surrounding circuit elements. This is significant since, with the exception of full ...

Keywords: CMOS ICs, VHDL, bridge defects, fault models, fault simulation, neural networks

7 Hierarchical physical design methodology for multi-million gate chips
Wei-Jin Dai

April 2001 **Proceedings of the 2001 international symposium on Physical design**
Full text available: pdf(136.52 KB) Additional Information: full citation, abstract, citings, index terms

In this paper, a design methodology for the implementation of multi-million gate system-on-chip designs is described.

Keywords: deep sub-micron, floorplanning, hierarchical design, partitioning, physical prototype, placement

8 An effective low powr design methodology based on interconnect prediction
Shih-Hsu Huang
March 2001 **Proceedings of the 2001 international workshop on System-level interconnect prediction**
Full text available: pdf(150.24 KB) Additional Information: full citation, abstract, references, index terms

The demand for low power digital systems has motivated significant research. However, the power estimation at the logic level is a difficult task because interconnect plays a role in determining the total chip power dissipation. As a result, the power optimization at the logic level may be inaccurate due to the lack of physical place and route information. In this paper, we will present an effective low power design methodology based on interconnect prediction at the logic level. The propos ...

9 Power and timing modeling for ASIC designs
W. Roethig, A. M. Zarkesh, M. Andrews
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(44.70 KB) Publisher Site Additional Information: full citation, references, index terms

10 A practical clock tree synthesis for semi-synchronous circuits
Masahiko Toyonaga, Kelichi Kurokawa, Takuya Yasui, Atsushi Takahashi
May 2000 **Proceedings of the 2000 international symposium on Physical design**
Full text available: pdf(163.92 KB) Additional Information: full citation, references, citings

Keywords: clock scheduling, clock-input timing, environmental and manufacturing conditions, semi-synchronous, various timing clock tree, zero skew clock tree

11 A sensitivity based placer for standard cells
Bill Halpin, C. Y. Roger Chen, Naresh Sehgal
March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**
Full text available: pdf(553.34 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a new timing driven method for global placement. Our method is based on the observation that similar net length reductions in the different nets that make up a path may not impact the path delay in the same way. For each net in the design, we compute the *net sensitivity*, or the path delay reduction as a result of net length improvements. We use very accurate delay models that include the impact of waveform slope and driver loading effects. Our new timing driven algorithm use ...

12 Vertical benchmarks for CAD

Christopher Inacio, Herman Schmit, David Nagle, Andrew Ryan, Donald E. Thomas, Yingfai Tong, Ben Klass
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(90.16 KB) Additional Information: full citation, references, index terms

13 Robust IP watermarking methodologies for physical design
Andrew B. Kahng, Stefanus Mantik, Igor L. Markov, Miodrag Potkonjak, Paul Tucker, Huijuan Wang, Gregory Wolfe
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(425.94 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Increasingly popular reuse-based design paradigms create a pressing need for authorship enforcement techniques that protect the intellectual property rights of designers. We develop the first intellectual property protection protocols for embedding design watermarks at the physical design level. We demonstrate that these protocols are tarnsparent with respect to existing industrial tools and design flows, and that they can embed watermarks into real-world industrial designs ...

Keywords: intellectual property test, system-on-chip test, testing embedded core

14 VAMP: a VHDL based concept for accurate modeling and post layout timing simulation of electronic systems
Bernhard Wunder, Gunther Lehmann, Klaus D. Müller-Glaser
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(330.37 KB) Additional Information: full citation, references, citings, index terms

15 VHDL & Verilog compared & contrasted—plus modeled example written in VHDL, Verilog and C
Douglas J. Smith
June 1996 **Proceedings of the 33rd annual conference on Design automation**
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1. **IEEE standard for standard delay format (SDF) for the electronic design process**
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2. **OLIVIA: object oriented logic simulation implementing the VITAL standard**
Fleischmann, J.; Schlagenhaft, R.; Peller, M.; Frohlich, N.;
VLSI, 1997. Proceedings. Seventh Great Lakes Symposium on
13-15 March 1997 Page(s):51 - 56
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3. **Delay and power calculation standards - Part 3: Standard Delay Format (SDF) for design process**
IEC 61523-3 First edition 2004-09; IEEE 1497
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